GP/2151

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TRANSMITTAL FORM

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Application Number	10/037,861	
Filing Date	January 2, 2002	No. of the Control of
First Named Inventor	Chong, Yan	RECEIVE
Group Art Unit	2151	APR 1 2 2002
Examiner Name	Unassigned	- Conto

015114-054810US Technology Cente 2100 Total Number of Pages 5 w/18 cited references Attorney Docket Number ENCLOSURES (check all that apply) After Allowance Communication to Assignment Papers Fee Transmittal Form (for an Application) Group Appeal Communication to Board of Fee Attached Drawing(s) Appeals and Interferences Appeal Communication to Group Amendment / Response Licensing-related Papers (Appeal Notice, Brief, Reply Brief) Petition Routing Slip (PTO/SB/69) After Final Proprietary Information and Accompanying Petition Petition to Convert to a Affidavits/declaration(s) Status Letter **Provisional Application** Power of Attorney, Revocation Other Enclosure(s) Extension of Time Request Change of Correspondence Address (please identify below): Terminal Disclaimer copies of 18 references Express Abandonment Request Request for Refund Return Postcard CD, Number of CD(s) with form PTO/SB/08B (3 pages) The Commissioner is authorized to charge any additional fees to Certified Copy of Priority Deposit Account 20-1430. Remarks Document(s) Response to Missing Parts/

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Incomplete Application

Response to Missing
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April 1, 2002

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Technology Center 2100

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Yan Chong et al.

Application No.: 10/037,861

Filed: January 2, 2002

For: SELF-COMPENSATING DELAY CHAIN FOR MULTIPLE-DATE-RATE

INTERFACES

BOX IDS

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

Examiner: Unassigned

Art Unit:

2151

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and

§1.98

The references cited on attached form PTO/SB/08B are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no

Yan Chong et al.

Application No.: 10/037,861

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representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that <u>no fee is required</u> for submission of this statement, since it is being submitted prior to the first Office Action. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

J. Matthew Zigmant/ Reg. No. 44,005

TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, 8th Floor San Francisco, California 94111-3834 Tel: 650-326-2400 Fax: 650-326-2422

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Substitute for form 1449B/PTO **Application Number** INFORMATION DISCLOSURE Filing Date TATEMENT BY APPLICANT **First Named Inventor**

Complete if Known 10/037,861 January 2, 2002 Chong, Yan Group Art Unit 2151 **Examiner Name** Unassigned 015114-054810Usechnology Cepter 2100 Attorney Docket Number

			U.S. PATENT DOCUM	MENTS	
		U.S. Patent Document			Pages, Columns, Lines,
Examiner Initials *	Cite No.1	Number Kind Code² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Where Relevant Passages or Relevant Figures Appear
	AA	5,555,214	Sung et al.	09-10-1996	
•	AB	5,633,830	Sung et al.	05-27-1997	
•	AC	5,764,080	Huang et al.	06-09-1998	
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	AM	6,252,419	Sung et al.	06-26-2001	

OTHER PRIOR ART NON PATENT LITERATURE DOCUMENTS				
Examiner Initials *	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²	
	AN	MICHAEL B. BENDAK et al., "CMOS VLSI Implementation of Gigabyte/Second Computer Network Links", IEEE, 1996, pp. 269-272		
	AO	"Virtex-II 1.5V Field-Programmable Gate Arrays", XILINX, DS031-2 (v1.5), April 2, 2001, pp. 1-36		
	AP	ANDREA BONI et al., "LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-μm CMOS" IEEE Journal of Solid-State Circuits, vol. 36, no. 4, April 2001, pp. 706-711		
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	AR	"APEX 20K Programmable Logic Device Family", Altera Corporation, May 2001, pp. 1-8, 37-47		

	 	
Examiner	Date	
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¹ Unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.